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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,664	03/29/2001	Li Xu	71795/11926	6159

24932 7590 08/10/2005

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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,664	XU ET AL.	
	Examiner	Art Unit	
	John L. Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,9-11,13-15,17 and 18-21* is/are rejected.

7)☒ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03292001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of prior claims 8, 10 pending rewriting in independent form including all of the limitations of the base claim and any intervening claims are withdrawn in view of the newly discovered reference(s) to Raychaudhuri et al. (Patent Number 5638371). Rejections based on the newly cited reference(s) follow.

Double Patenting

2. Claim 22 is objected to under 37 CFR 1.75 as being a duplicate of claim 20. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6, 9, 11, 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Raychaudhuri et al. (Patent Number 5638371).

Claim 1, Raychaudhuri teaches a payload data unit switching engine (FIG. 4, column 6 lines 19-34, FIG. 5) referenced by the Core MAC Processor 102 for data exchange with the DLC 103 of the ATM layer for switching wherein the payload is the ATM 48 Byte Payload, of a payload data unit switching node (FIG. 2, column 4 lines 54-65) referenced by the Base Station 38 for switching ATM cell with the ATM Based Switching Network 44, the switching engine comprising a payload data unit traffic management database (FIG. 6, column 10 lines 4-14) referenced by the Frame Schedule Table 134, a payload data unit traffic management processor performing intensive traffic management computations in ensuring guaranteed levels of service (FIG. 4, Abstract lines 10-18, FIG. 5, column 1 lines 6-14) referenced by the Base Station Supervisory MAC Processor 101 for MAC frame allocation of ATM ABR VBR and CBR each representative of a quality of service selection, and updating the payload data unit traffic management database (FIG. 7) referenced by Step 178 the Update Virtual Circuit to Slot Table of Core MAC, a payload data unit switching processor switching payload data unit traffic based on switching database entries subject to payload data unit traffic

shaping criteria held in the traffic management database (FIG. 6) referenced by the Core MAC Processor Controller 136 which determines I/O Instruction According to Virtual Circuit # I/O Type and Slot # of Each Entry in the Table, and notification means for notifying the payload data unit switching processor of an update of the payload data unit traffic management database (FIG. 7, column 10 lines 22-32) referenced by the MAC Supervisory Processor notifiying the Core MAC via a update of the VC to Slot Table of Core MAC step 178.

Claim 6, Raychaudhuri teaches wherein the notification means further comprises information exchange means enabling communication between the payload data unit switching processor and the payload data unit traffic management processor within the payload data unit switching node (FIG. 4, FIG. 7, column 10 lines 22-32) referenced by the notification Step 178 performed by the MAC Supervisory Processor 101 to the Core Processor 102 wherein both processors are in the ATM Base Station node 100.

Claim 9, Raychaudhuri teaches wherein the information exchange means includes a working store (FIG. 6, column 9 lines 44-49) referenced by the storage of information in the Frame Schedule Table 134 which is a working updatable memory store of an information exchange through scheduling.

Claim 11, Raychaudhuri teaches wherein the payload data unit traffic management processor includes the working store (FIG. 4, FIG. 6) referenced by the working store

memory of the Frame Schedule Table 134 within the Core MAC Processor of the Base Station MAC 100.

Claim 17, Raychaudhuri teaches wherein the information exchange means further comprises at least one dedicated data bus for communication between the payload data unit switching processor and the payload data unit traffic management processor (FIG. 4, column 6 lines 19-34) referenced by the Control Channel between the Core MAC Process 102 and the Base Station Supervisory MAC 101.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri as applied to claim 1 above, in view of Rao (Patent Number 6789118).

Claim 2, Raychaudhuri teaches an ATM system for assignment of slots based on ATM traffic shaper parameters. Raychaudhuri does not teach a payload data unit traffic management database stores resource utilization information.

Rao teaches a data traffic management database (column 2 lines 23-29) referenced by the call policy database, stores resource utilization information (FIG. 3, column 9 lines 4-15) referenced by the call policy parameters comparison to resource utilization, the resource utilization information specifying a current state of the data traffic conveyed by the data switching node (column 9 lines 16-22) referenced by the QoS level specifying the current state of the data traffic.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the QoS call policy parameters of Rao to the payload MAC services ATM system of Raychaudhuri for the purpose of identifying a characteristic of the connection request and selects a router based on the identified characteristic as suggested by Rao (column 2 lines 23-26).

Claim 3, Raychaudhuri teaches an ATM system for assignment of slots based on ATM traffic shaper parameters. Raychaudhuri does not teach resource utilization information is stored in bit encoded form.

Rao teaches wherein the resource utilization information is stored in a bit encoded form (FIG. 11, FIG. 13) referenced by the Call Policy Record which is bit encoded in a database.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the QoS call policy parameters of Rao to the payload MAC services ATM system of Raychaudhuri for the purpose of identifying a characteristic of the connection request and selects a router based on the identified characteristic as suggested by Rao (column 2 lines 23-26).

Claim 4, Raychaudhuri teaches an ATM system for assignment of slots based on ATM traffic shaper parameters. Raychaudhuri does not teach data traffic shaping criteria includes data traffic shaping heuristics.

Rao teaches wherein the data traffic shaping criteria includes data traffic shaping heuristics (FIG. 11, column 14 lines 48-67, column 15 lines 1-8) referenced by the call policy record definition of QoS level in conjunction with the Quality of Access level to control traffic shaping heuristics, enabling the data switching processor to enforce service level guarantee data traffic constraints on data traffic flows processed by the data switching node (FIG. 13, column 1 lines 26-35, column 16 lines 4-38) referenced by service level guaranteed implemented by the QoS access thresholds in determining data packets to forward and switch.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the QoS call policy parameters of Rao to the payload MAC services ATM system of Raychaudhuri for the purpose of identifying a characteristic of the connection request and selects a router based on the identified characteristic as suggested by Rao (column 2 lines 23-26).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri as applied to claims 1, 6, 9 above, in view of Zigras (Patent Number 5978889).

Claim 10, Raychaudri teaches an ATM system for assignment of slots based on ATM traffic shaper parameters using a switching core processor and a traffic supervisory processor. Raychaudhuri does not teach the working store comprises mulit-ported random access memory.

Zigras teaches a working store comprises multi-ported random access memory enabling concurrent access thereto by the switching processor and the traffic management processor (column 1 lines 65-67, column 4 lines 1-20, FIG. 3, column 5 lines 25-35) referenced by the concurrent processing of Quad Port RAM 43 accessible by the Digital Signal Processor 49 which is a core processor and the I/O device 45 which is the supervisory processor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multiport memory of Zigras to the payload MAC services ATM system of Raychaudhuri for the purpose of to avoid waiting in a memory when multiple data transferring devices in excess of 2 need access to the memory as suggested by Zigras (column 1 lines 48-50).

Claims13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri as applied to claims 1, 6 above, in view of Gasbarro et al. (Patent No. 2002/0071450).

Claim 13, Raychaudhuri teaches an ATM system for assignment of slots based on ATM traffic shaper parameters using a switching core processor and a traffic supervisory processor. Raychaudhuri does not teach the information exchange means includes data registers internally associated with the payload data unit switching processor. Gasbarro teaches an information exchange means includes data registers internally associated with the payload data unit switching processor (FIG. 4B, FIG. 7, page 7 paragraphs [0054]-[0056]) referenced by the Micro Controller Subsystem 700 associated with the Host-Fabric Adaptor 120 performing switching of the fabric 100' wherein the Micro Engine uses micro registers for data supplies by interface blocks, the data registers storing at least a portion of the payload data unit traffic management database (FIG. 7, page 7 paragraph [0057]) referenced by the memory mapped register including HCA context registers for control status for information transfer.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the host fabric adaptor system of Gasbarro to the payload MAC services ATM system of Raychaudhuri for the purpose of connecting a bandwidth

optimized with minimal area vertical sliced memory architecture of a host system to a channel-based switched fabric in a data network as suggested by Gasbarro (page 1 paragraph [0001]).

Claim 15, Raychaudhuri teaches wherein the information exchange means includes a communications protocol (FIG. 5) referenced by the TDMA MAC frame including ATM communications protocol, the communications protocol including direct memory writes to the data registers on updating the payload data unit traffic management database (FIG. 4, FIG. 6) referenced by the Core MAC Process 102 interface to the DLC of the ATM Layer for Channel Request whereby the Base Station Supervisory MAC updates the Frame Schedule Table 134.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri and Gasbarro as applied to claims 1, 6, 13 above, in further view of Zigras (Patent Number 5978889).

Claim 14, Raychaudri and Gasbarro teach an ATM system for assignment of slots based on ATM traffic shaper parameters using a switching core processor and a micro

engine using registers. Raychaudhuri and Gasbarro do not teach the data registers comprises mulit-ported random access memory.

Zigras teaches data registers comprise multi-ported random access memory enabling concurrent access thereto by the switching processor and the traffic management processor (column 1 lines 65-67, column 4 lines 1-20, FIG. 3, column 5 lines 25-35, Fig. 5, column 8 lines 44-52) referenced by the Page Register 129 controlling the memory of the concurrent processing of Quad Port RAM 43 accessible by the Digital Signal Processor 49 which is a core processor and the I/O device 45 which is the supervisory processor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multiport memory of Zigras to the payload MAC services ATM system of Raychaudhuri and Gasbarro for the purpose of to avoid waiting in a memory when multiple data transferring devices in excess of 2 need access to the memory as suggested by Zigras (column 1 lines 48-50).

Claims 18, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri, in view of Johnson et al. (Pub. No. US 2002/0133593).

Claim 18, Raychaudhuri teaches a method for data traffic flows conveyed by a multiport data switching node (FIG. 2) referenced by the Base Station 38 with the ATM Network Interface Unit 42 as a multiport switch for data traffic flows, the method comprising of extracting header information from a Payload Data Unit (PDU) received by a switching processor from an input port of the data switching node (FIG. 4, FIG. 5) referenced by the TDMA MAC frame including a Wireless Header of the ATM payload received at the Core MAC Process 102 from the PHY RX 109 port, querying a switching database to determine an output port to forward the PDU (FIG. 6, column 10 lines 4-14) referenced by the Core MAC Processor accessing the Frame Schedule Table 134 in determination of the Transmit Cells/Pkts on Allocated Slots #s 144, querying a data traffic management database maintained by a data traffic management processor (FIG. 6) referenced by the update of the Frame Schedule Table 134 by signals From Supervisory MAC Processor, the data traffic management database storing data traffic management information (FIG. 6) referenced by the Frame Schedule Table 134 storing entries for Virtual Circuit and I/O Type and Slot #, processing the PDU subject to data traffic constraints and current states of the data traffic flows included in the data traffic management information (FIG. 6, Fig. 7, column 10 lines 22-32) referenced by the traffic constraint of Slot Allocation Received for Virtual Circuit (i) step 174 followed by current state of Update of the Virtual Circuit to Slot information of the Table of Core MAC step 178 to determine the transmit cell slot allocation, updating the data traffic management database upon computing a current state of the data traffic flows (FIG. 7) referenced by

the MAC Supervisory Processor Update VC to Slot mapping of the Table of Core MAC step 178 based on the current state slot allocation. Raychaudhuri does teach not enforcing service level agreements nor selectively providing feedback information to the data traffic management processor.

Johnson teaches enforcing service level agreements (page 20 paragraph [0165]) referenced by the SLA based parameters of the service request, selectively providing feedback information to the data traffic management processor regarding actions taken by the switching processor in processing the PDU (FIG. 1A, page 12 paragraphs [0098]-[0099]) referenced by the flow control feedback to prevent congestion of the processor engine based on the movement of specific data type into system memory.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the resource information management system of Johnson to the payload MAC services ATM system of Raychaudhuri for the purpose of increased performance and improved predictability of computing systems in the performance of designated tasks across a wide range of loads as suggested by Johnson (page 1 paragraph [0005]).

Claim 21, Raychaudhuri teaches an ATM system for assignment of slots based on ATM traffic shaper parameters. Raychaudhri does not teach querying a service level agreement database to determine service level guarantees.

Johnson teaches wherein computing the current state of the data traffic flows the method further comprises the step of querying a service level agreement database

associated with the traffic management processor to determine the service level guarantees (FIG. 2, page 7 paragraphs [0065]-[0066], FIG. 5, page 20 paragraphs [0165]-[0166]) referenced by the evaluation of resources based on SLA information from the memory of the Storage Subsystem 210.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the resource information management system of Johnson to the payload MAC services ATM system of Raychaudhuri for the purpose of increased performance and improved predictability of computing systems in the performance of designated tasks across a wide range of loads as suggested by Johnson (page 1 paragraph [0005]).

Claims 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raychaudhuri and Johnson as applied to claim 18 above, and further in view of Rao (Patent No. 6789118).

Claim 19, Raychaudhuri and Johnson teach an ATM system for assignment of slots based on ATM traffic shaper parameters and congestion control. Raychaudhuri and Johnson do not teach processing PDU subject to data traffic shaping heuristics.

Rao teaches wherein processing the PDU the method further comprises a step of processing the PDU subject to data traffic shaping heuristics (FIG. 11, column 14 lines 36-67, column 15 lines 1-8) referenced by the call policy record definition of QoS level in conjunction with the Quality of Access level to control traffic shaping heuristics and determine the routing of the packet based on call-policy, providing data traffic flow control for the input port (FIG. 13, FIG. 16,column 18 lines 48-65) referenced by the QoA level mapped to Access Threshold for determination of the resource to be allocated to a port.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the QoS call policy parameters of Rao to the payload MAC services ATM system of Raychaudhuri and Johnson for the purpose of identifying a characteristic of the connection request and selects a router based on the identified characteristic as suggested by Rao (column 2 lines 23-26).

Claim 20, Raychaudhuri and Johnson teach an ATM system for assignment of slots based on ATM traffic shaper parameters and congestion control. Raychaudhuri and Johnson do not teach processing PDU subject to data traffic shaping heuristics.

Rao teaches wherein processing the PDU the method further comprises a step of processing the PDU subject to data traffic shaping heuristics (FIG. 11, column 14 lines 36-67, column 15 lines 1-8) referenced by the call policy record definition of QoS level in conjunction with the Quality of Access level to control traffic shaping heuristics and determine the routing of the packet based on call-policy, providing data traffic flow

control for the output port (FIG. 13, FIG. 16,column 18 lines 48-65) referenced by the QoA level mapped to Access Threshold for determination of the resource to be allocated to a port.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the QoS call policy parameters of Rao to the payload MAC services ATM system of Raychaudhuri and Johnson for the purpose of identifying a characteristic of the connection request and selects a router based on the identified characteristic as suggested by Rao (column 2 lines 23-26).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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